SONY

CXA2089Q/S

S2-Compatible 5-Input 2-Output Audio/Video Switch

Description

The CXA2089Q/S is a 5-input, 2-output audio/video switch featuring I^2C bus compatibility for TVs. This IC has input pins that are compatible with S2 protocol.

Features

- 3 inputs that are compatible with S2 protocol
- Serial control with I^2C bus
- 5 inputs, 2 outputs
- The desired inputs can be selected independently for each of the 2 outputs
- Wide band video amplifier (20MHz, –3dB)
- Y/C MIX circuit
- Slave address can be changed (90H/92H)
- Audio muting from external pin
- High impedance maintained by I^2C bus lines (SDA, SCL) even when power is OFF
- Wide audio dynamic range (3Vrms typ.)

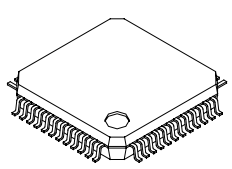
Applications

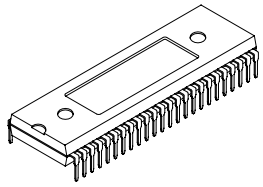
Audio/video switch featuring I^2C bus compatibility for TVs

Structure

Bipolar silicon monolithic IC

CXA2089Q	CXA2089S
48 pin QFP (Plastic)	48 pin SDIP (Plastic)





Absolute Maximum Ratings

• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1500	mW

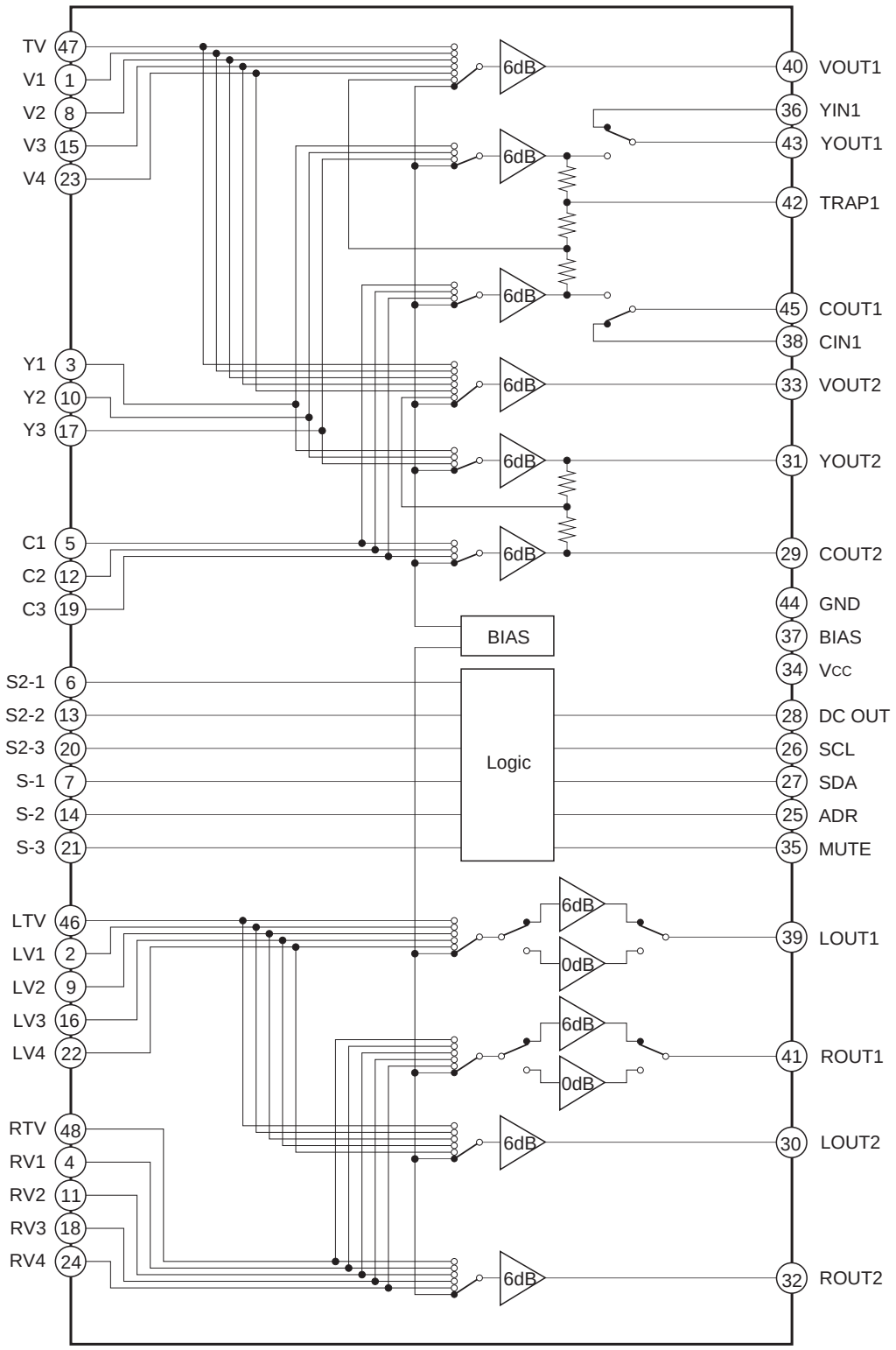
Operating Conditions

Supply voltage	9 ± 0.5	V

E97431B7Z-PS

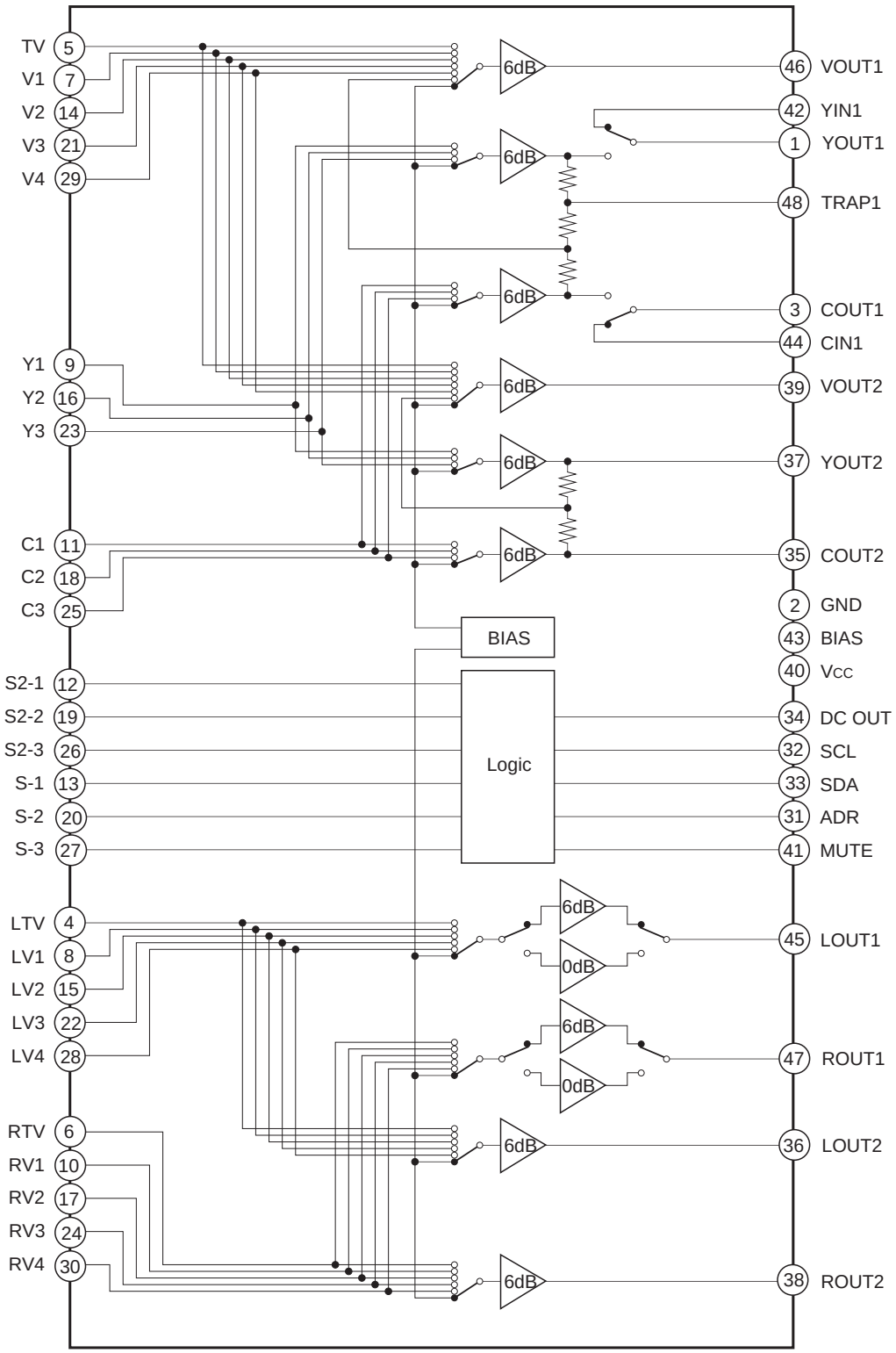
Block Diagram

CXA2089Q



Audio system is attenuated by 6dB for 6kΩ resistor input, and a total gain is 0dB (LOUT1 and ROUT1 can be changed to –6dB).

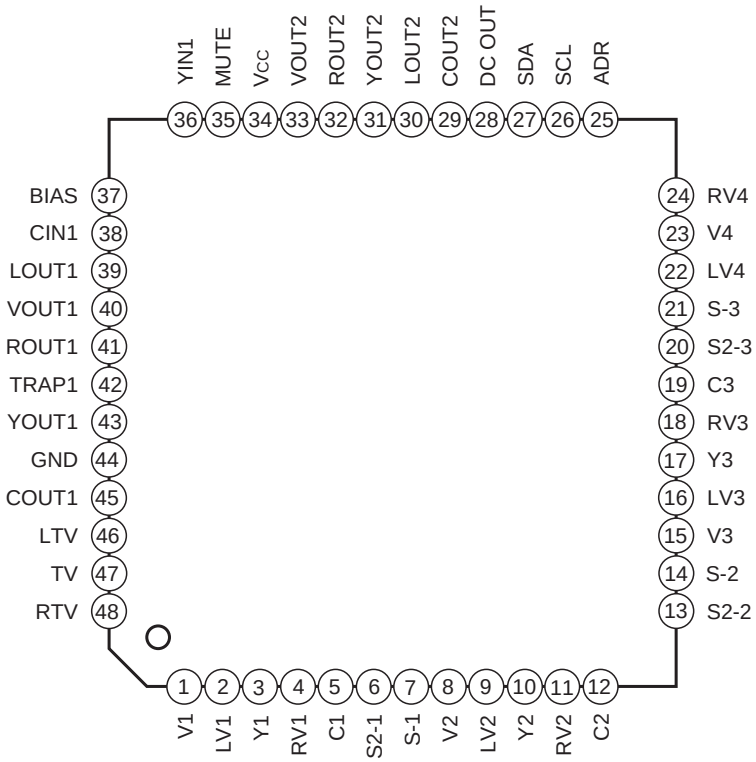
CXA2089S



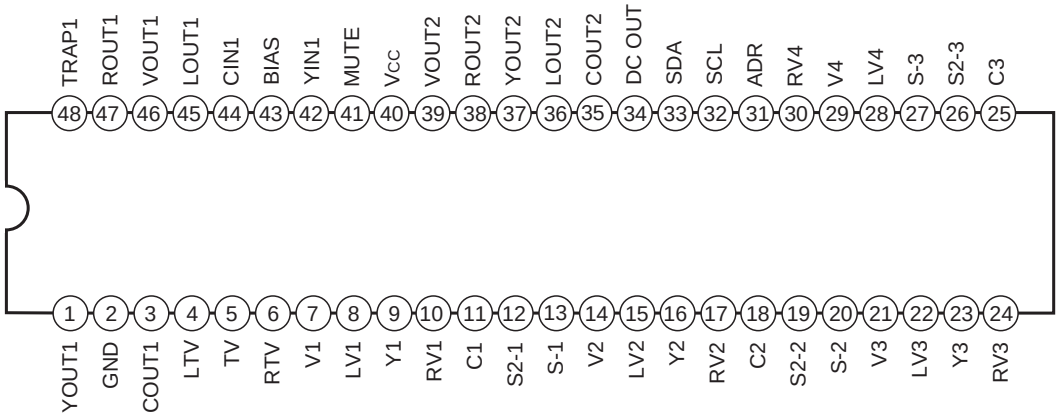
Audio system is attenuated by 6dB for 6kΩ resistor input, and a total gain is 0dB (LOUT1 and ROUT1 can be changed to –6dB).

Pin Configuration

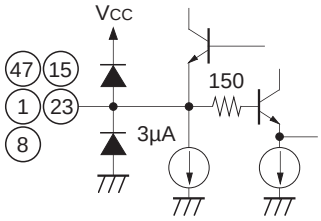
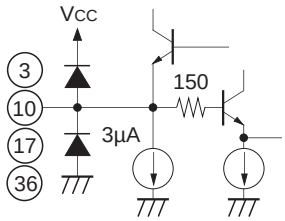
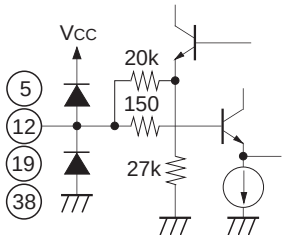
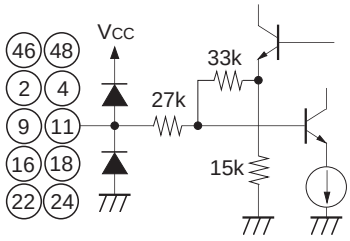
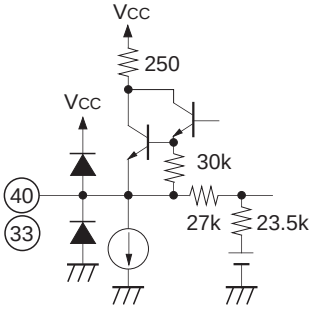
CXA2089Q

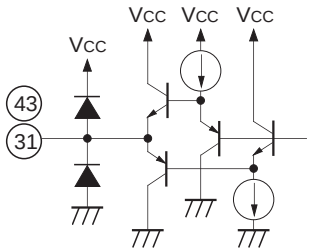
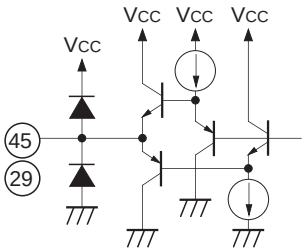
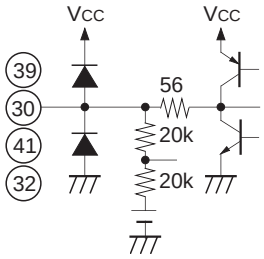
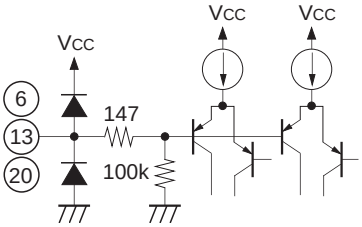
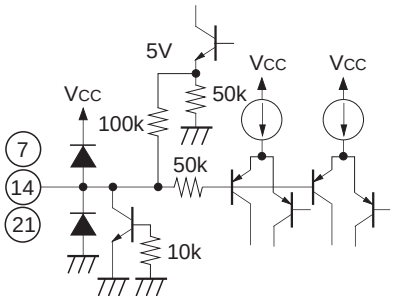
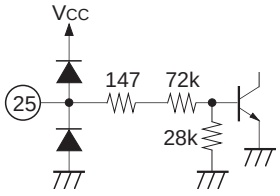


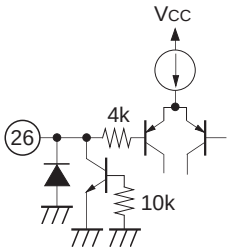
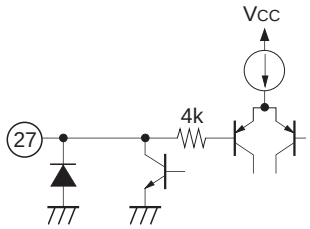
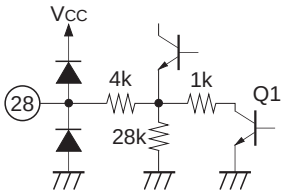
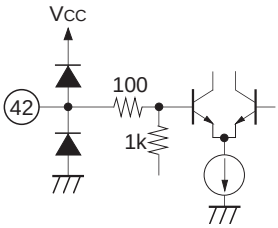
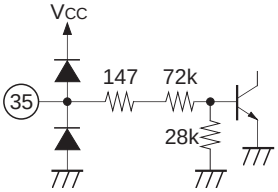
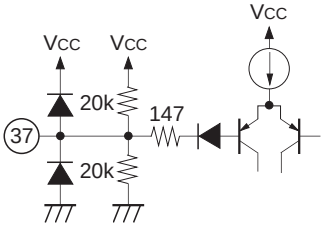
CXA2089S



Pin Description Pin numbers in brackets are for the CXA2089S.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
47 (5) 1 (7) 8 (14) 15 (21) 23 (29)	TV V1 V2 V3 V4	4.0V		Video signal inputs. Input composite video signals.
3 (9) 10 (16) 17 (23) 36 (42)	Y1 Y2 Y3 YIN1	4.0V		Y/C separation signal inputs. Input luminance signals. The YIN1 pin inputs the signal obtained by Y/C separating the VOUT1 pin output.
5 (11) 12 (18) 19 (25) 38 (44)	C1 C2 C3 CIN1	4.5V		Y/C separation signal inputs. Input chrominance signals. The CIN1 pin inputs the signal obtained by Y/C separating the VOUT1 pin output.
46 (4) 2 (8) 9 (15) 16 (22) 22 (28) 48 (6) 4 (10) 11 (17) 18 (24) 24 (30)	LTV LV1 LV2 LV3 LV4 RTV RV1 RV2 RV3 RV4	4.5V		Audio signal inputs.
40 (46) 33 (39)	VOUT1 VOUT2	3.9V		Video signal outputs. Output composite video signals.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
43 (1)	YOUT1	3.3V		Video signal outputs. Output luminance signals.
31 (37)	YOUT2	3.5V		
45 (3) 29 (35)	COUT1 COUT2	4.5V		Video signal outputs. Output chrominance signals.
39 (45) 30 (36) 41 (47) 32 (38)	LOUT1 LOUT2 ROUT1 ROUT2	4.5V		Audio signal outputs. Zo = 50Ω (within DC ± 2mA)
6 (12) 13 (19) 20 (26)	S2-1 S2-2 S2-3	—		Detects the S2-compatible DC superimposed onto the C signal. 4:3 video signal at 1.3V or less 4:3 letter-box signal at 1.3V or more to 2.5V or less 16:9 picture squeezed signal at 2.5V or more These pins are pulled down to GND by a 100kΩ resistor, so the 4:3 video signals are selected when open.
7 (13) 14 (20) 21 (27)	S-1 S-2 S-3	—		Composite video/S selector. The detection results are written to the status register. S signal at 3.5V or less Composite video signal at 3.5V or more These pins are pulled up to 5V by a 100kΩ resistor, so the composite video signals are selected when open.
25 (31)	ADR	—		Selects the slave address for the I^2C bus. 90H at 1.5V or less 92H at 2.5V or more 90H when open

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
26 (32)	SCL	—		I²C bus signal input VILmax = 1.5V VIHmin = 3.0V
27 (33)	SDA	—		I²C bus signal input VILmax = 1.5V VIHmin = 3.0V VOLmax = 0.4V
28 (34)	DC OUT	—		Outputs the S2-compatible DC superimposed onto the COUT2 output. The DC is superimposed by connecting this pin to the COUT2 output via a capacitor. Control is performed by the I²C bus. When 0V is output, Q1 is ON and the impedance is 5kΩ. S2 protocol output DC impedance of 10 ± 3kΩ is realized by attaching external resistance of 4.7kΩ. DC OUT (bus) Output DC 0 4.5V 1 0V 2 1.9V 3 4.5V
42 (48)	TRAP1	3.8V		Connects trap circuit for subcarrier.
35 (41)	MUTE	—		Audio signal output mute. Mute OFF at 1.5V or less Mute ON at 2.5V or more Mute OFF when open
37 (43)	BIAS	4.5V		Internal reference bias (Vcc/2). Connects to GND via a capacitor.

Electrical Characteristics (Ta = 25°C, V_{CC} = 9V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	No signal, no load	30	45	62	mA

Video system (Measurement circuit; Fig. 1)

Gain	GVv	f = 100kHz, 0.3Vp-p input	5.9	6.4	6.9	dB
Frequency response characteristics	FBWv1	f = 100kHz, input frequency where output amplitude is –3dB with 0.3Vp-p output serving as 0dB	15	20	—	MHz
Frequency response characteristics (Y/C mix)	FBWv2		10	15	—	MHz
Input dynamic range	Ddv	f = 100kHz, maximum with distortion < 1.0%	1.4	—	—	Vp-p
Cross talk	Vctv	f = 4.43MHz, 1Vp-p input	—	—	–50	dB

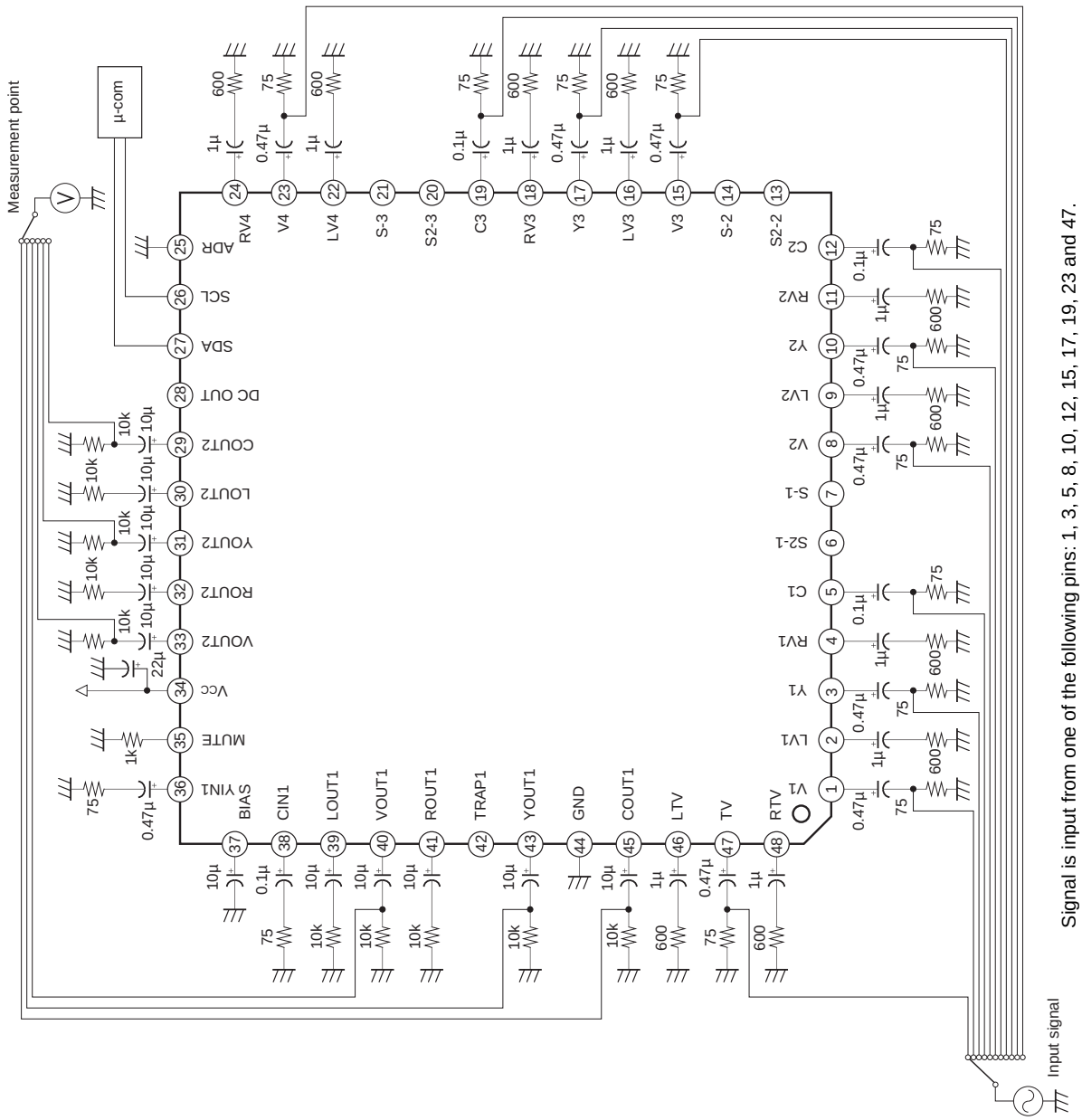
Audio system (Measurement circuits; Fig. 2 to Fig. 5)

Gain	GV_A	f = 1kHz, 1Vp-p input, 5.7kΩ resistor inserted to input	–1	0	1	dB
Frequency response characteristics	FBW_A	f = 1kHz, input frequency where output amplitude is –3dB with 1Vp-p output serving as 0dB	50	—	—	kHz
Total harmonic distortion	THD	f=1kHz, 2.2Vp-p input, where 400Hz HPF + 80kHz LPF are inserted	—	0.03	0.05	%
Input dynamic range	Dd_A	f=1kHz, maximum with distortion < 0.3%	2.8	3.0	—	Vrms
Cross talk	Vct_A	f=1kHz, 1Vp-p input	—	–90	–80	dB
Ripple rejection ratio	Vct_A	f=100Hz, 0.3Vp-p applied to Vcc	—	–55	–40	dB
Output DC offset	Voff	Offset voltage between input and output	–30	—	30	mV
Residual noise	VN_A	When 400Hz HPF+ 30kHz LPF are inserted	0	20	30	µVrms
S/N ratio	S/N	f=1kHz, 1Vrms input When 400Hz HPF + 30kHz LPF are inserted		–100	–90	dB

Logic system

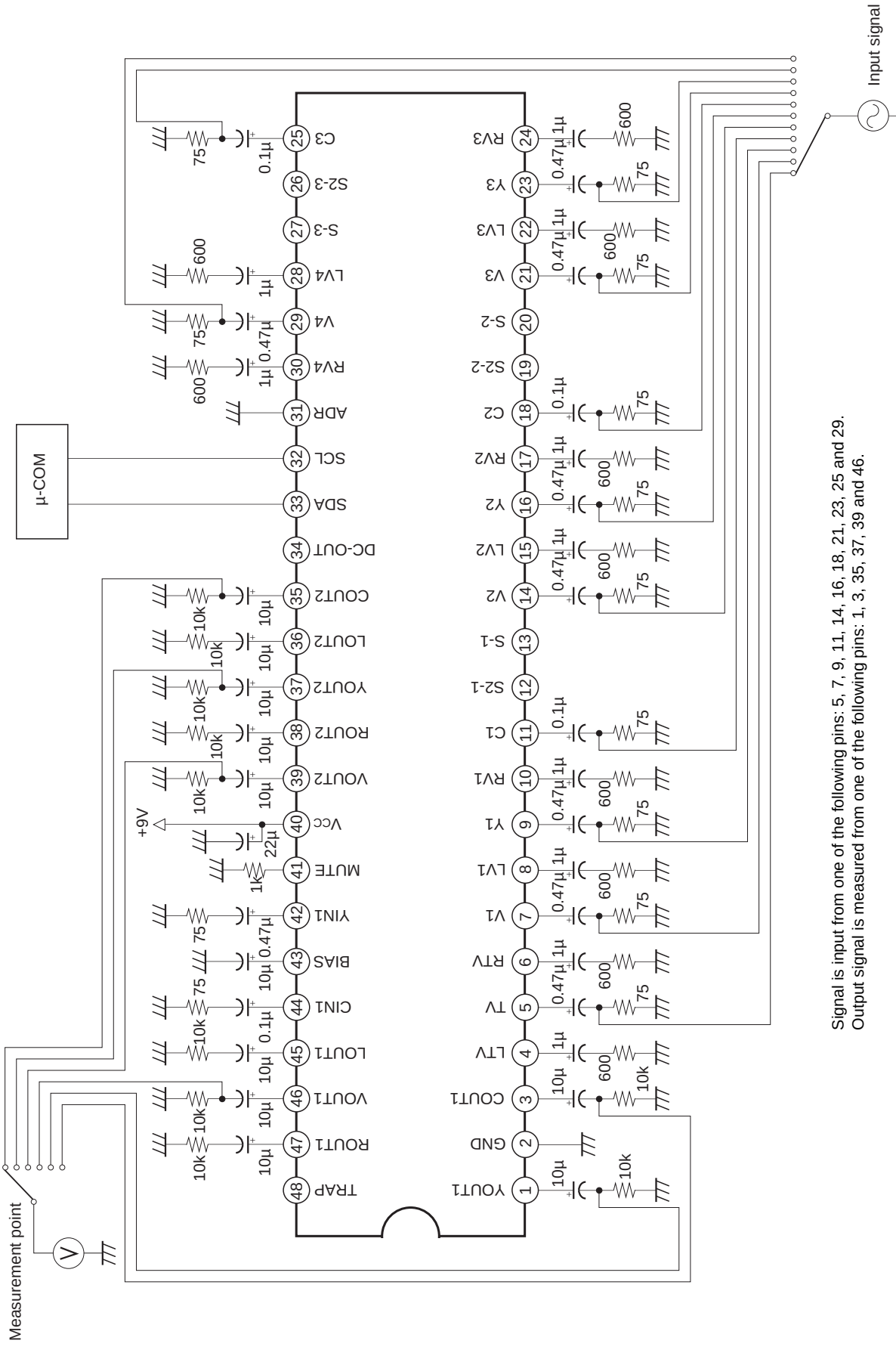
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		3.0	—	5.0	V
Low level input voltage	V_{IL}		0	—	1.5	V
Low level output voltage	V_{OL}	With SDA 3mA current supplied	0	—	0.4	V
High level input current	I_{IH}	V_{IH} = 4.5V	0	—	10	µA
Low level input current	I_{IL}	V_{IL} = 0.4V	0	—	10	µA
Maximum clock frequency	f_{SCL}		0	—	100	kHz
Minimum waiting time for data change	t_{BUF}		4.7	—	—	µs
Minimum waiting time for data transfer start	$t_{HD;STA}$		4.0	—	—	µs
Low level clock pulse width	t_{LOW}		4.7	—	—	µs
High level clock pulse width	t_{HIGH}		4.0	—	—	µs
Minimum waiting time for start preparation	$t_{SU;STA}$		4.7	—	—	µs
Minimum data hold time	$t_{HD;DAT}$		150	—	—	ns
Minimum data preparation time	$t_{SU;DAT}$		0	—	—	ns
Rise time	t_R		—	—	1	µs
Fall time	t_F		—	—	300	ns
Minimum waiting time for stop preparation	$t_{SU;STO}$		4.7	—	—	µs

Electrical Characteristics Measurement Circuit



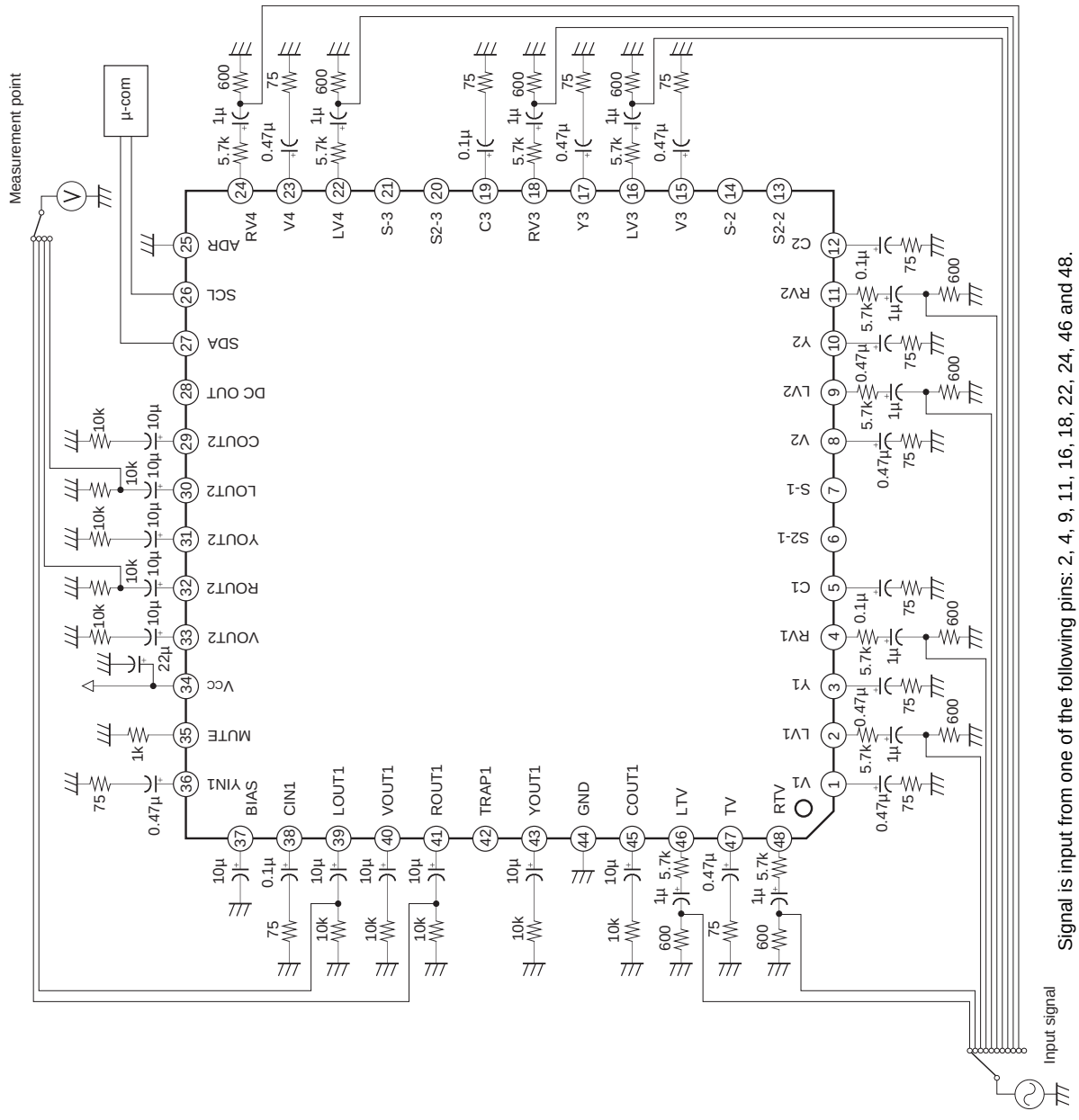
Signal is input from one of the following pins: 1, 3, 5, 8, 10, 12, 15, 17, 19, 23 and 47.
Output signal is measured from one of the following pins: 29, 31, 33, 40, 43 and 45.

Fig. 1-a. Video system (gain, frequency response characteristics, input dynamic range, cross talk) measurement circuit (CXA2089Q)



Signal is input from one of the following pins: 5, 7, 9, 11, 14, 16, 18, 21, 23, 25 and 29.
Output signal is measured from one of the following pins: 1, 3, 35, 37, 39 and 46.

Fig. 1-b. Video system (gain, frequency response characteristics, input dynamic range, cross talk) measurement circuit (CXA2089S)



Signal is input from one of the following pins: 2, 4, 9, 11, 16, 18, 22, 24, 46 and 48.
Output signal is measured from one of the following pins: 30, 32, 39 and 41.

Fig. 2-a. Audio system (gain, frequency response characteristics, total harmonic distortion, input dynamic range, cross talk) measurement circuit (CXA2089Q)

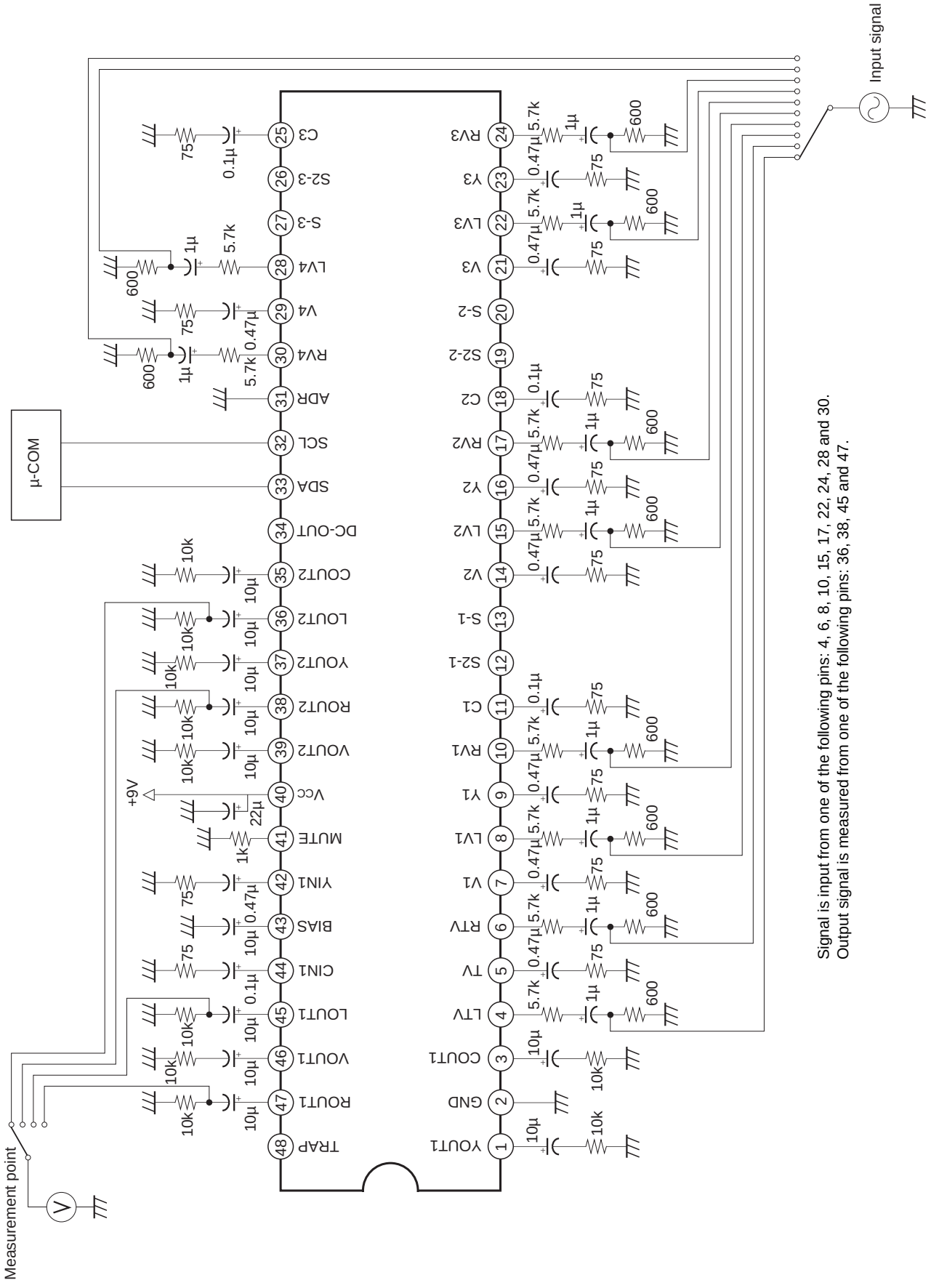
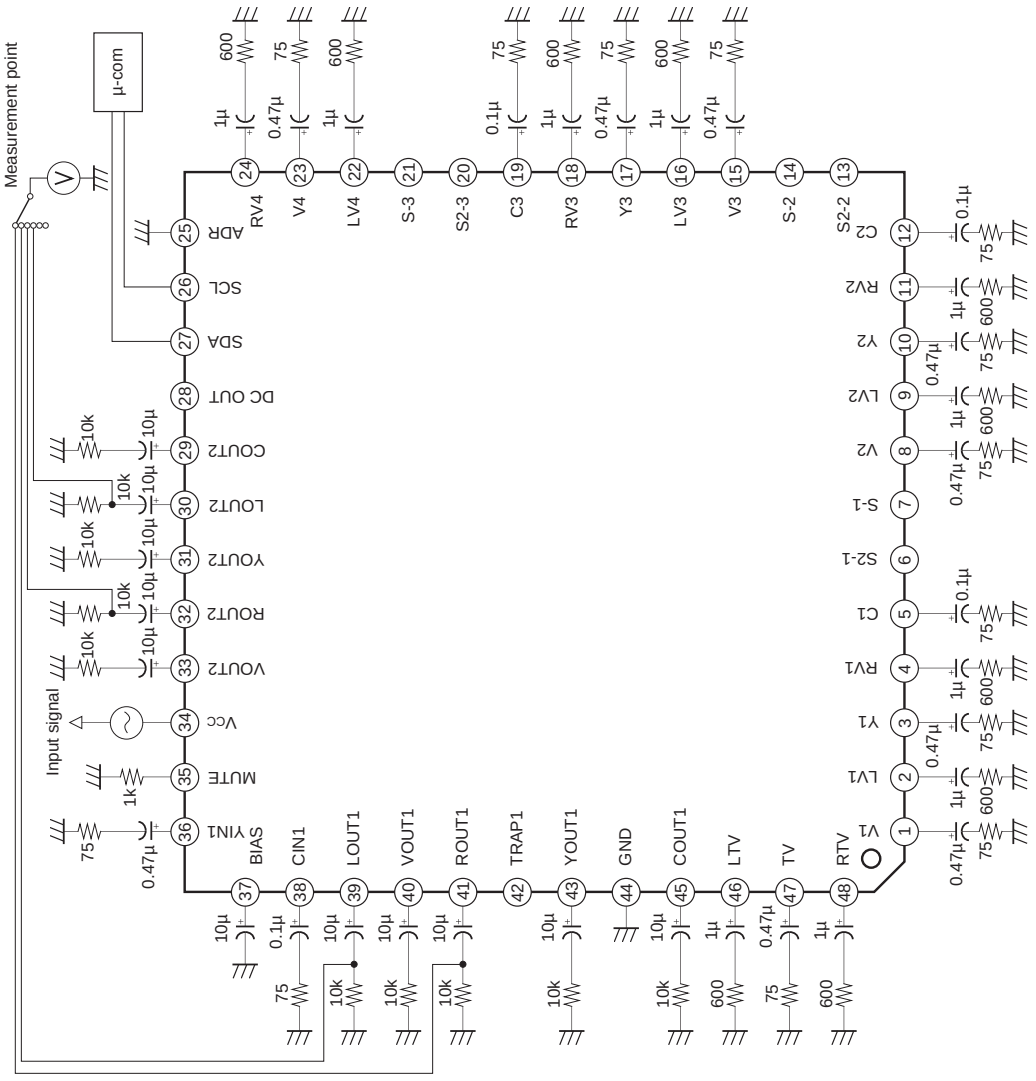
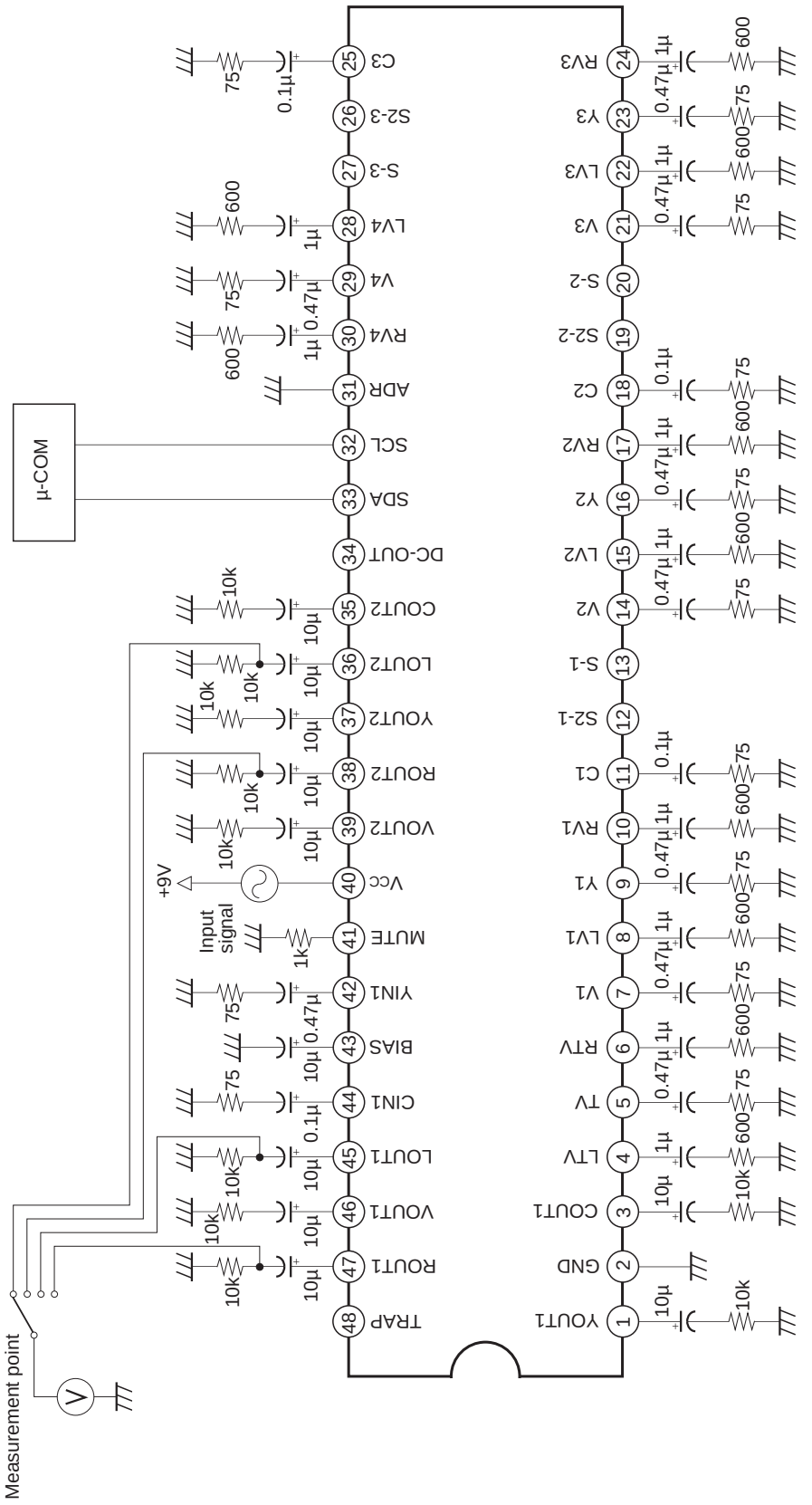


Fig. 2-b. Audio system (gain, frequency response characteristics, total harmonic distortion, input dynamic range, cross talk) measurement circuit (CXA2089S)



A f=100Hz, 0.3Vp-p signal is applied to Vcc and the output signals from Pins 30, 32, 39 and 41 are measured.

Fig. 3-a. Audio system (ripple rejection ratio) measurement circuit (CXA2089Q)



A f=100Hz, 0.3Vp-p signal is applied to Vcc and the output signals from Pins 36, 38, 45 and 47 are measured.

Fig. 3-b. Audio system (ripple rejection ratio) measurement circuit (CXA2089S)

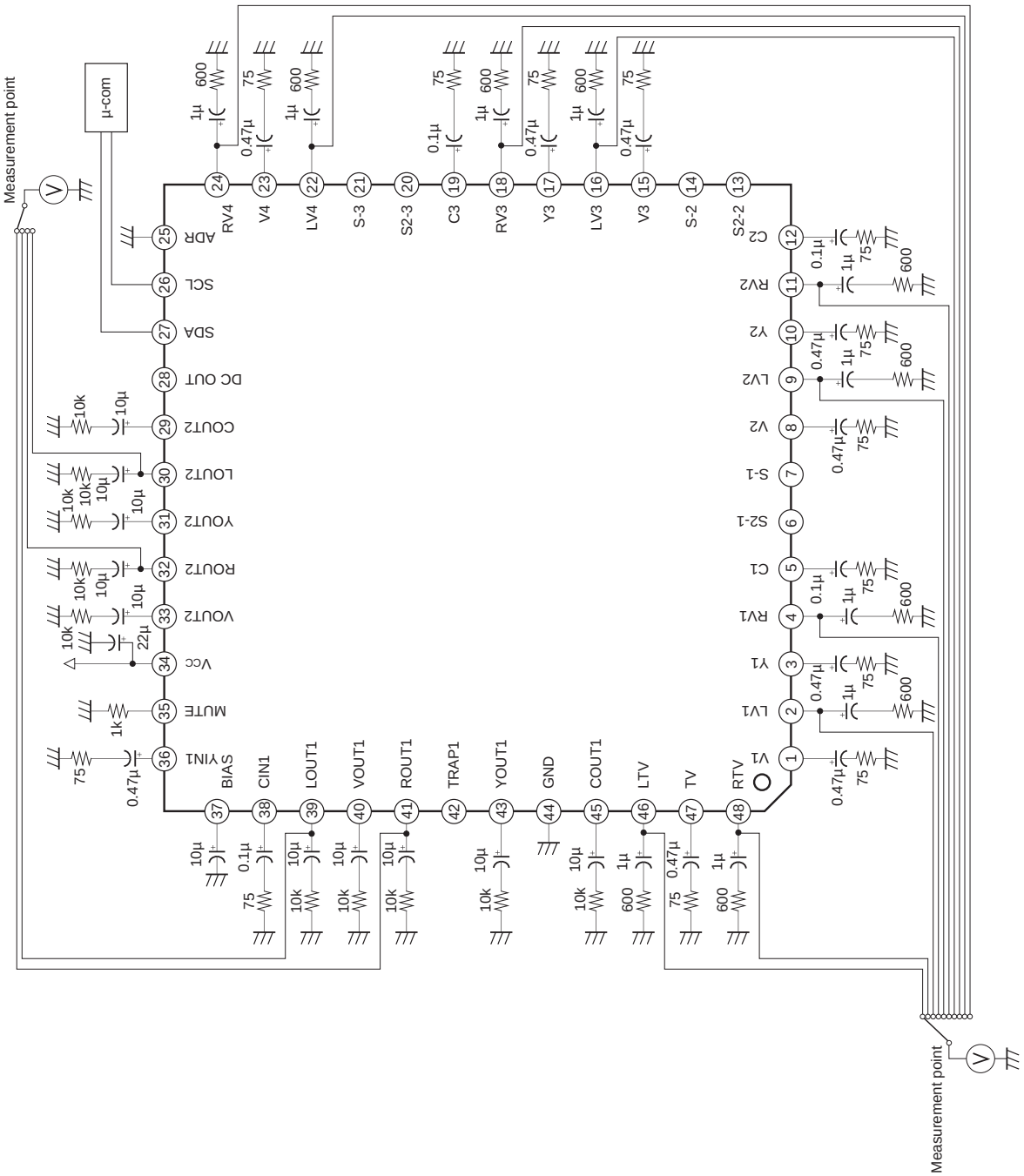


Fig. 4-a. Audio system (output DC offset voltage) measurement circuit (CXA2089Q)

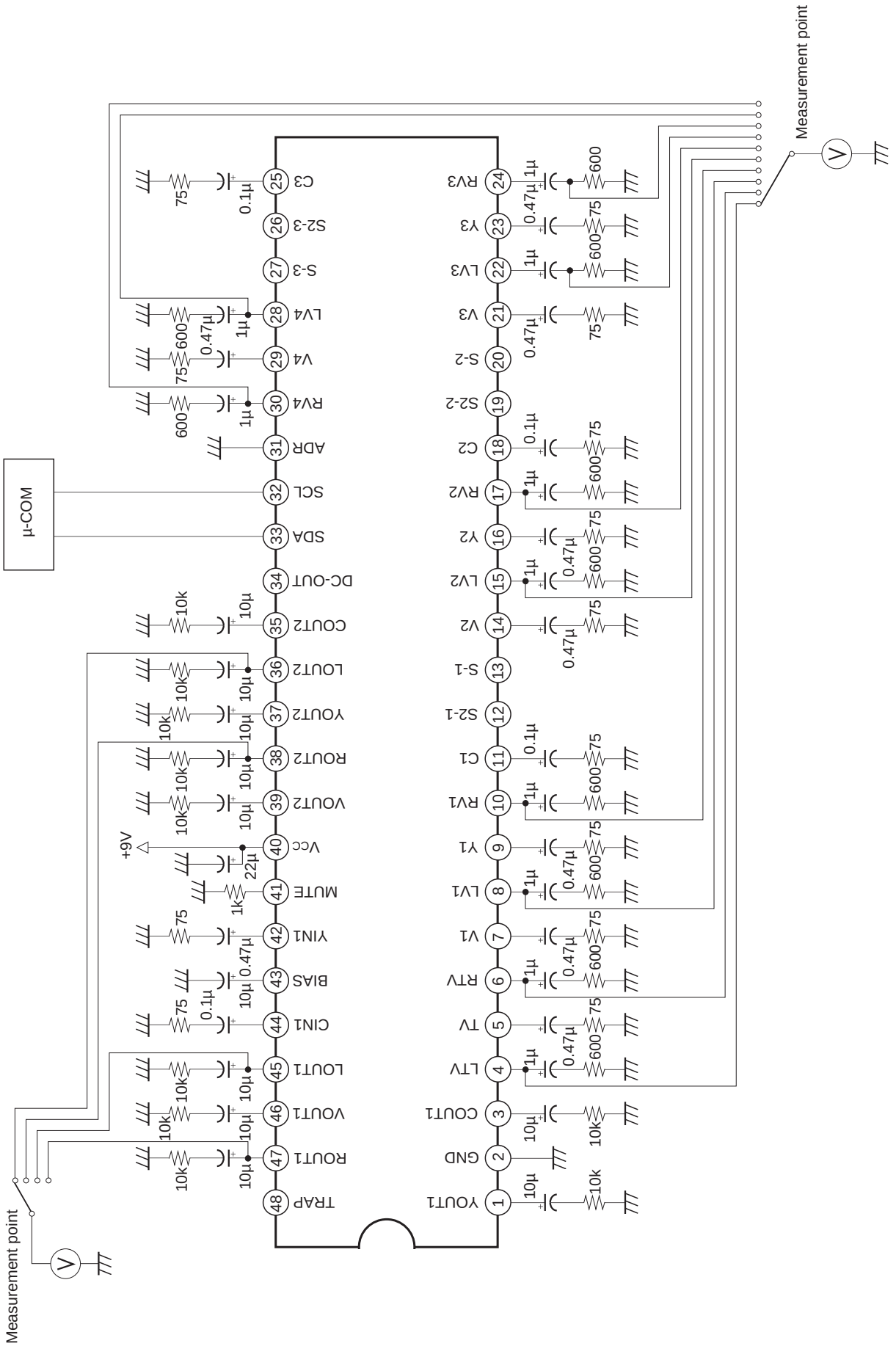


Fig. 4-b. Audio system (output DC offset voltage) measurement circuit (CXA2089S)

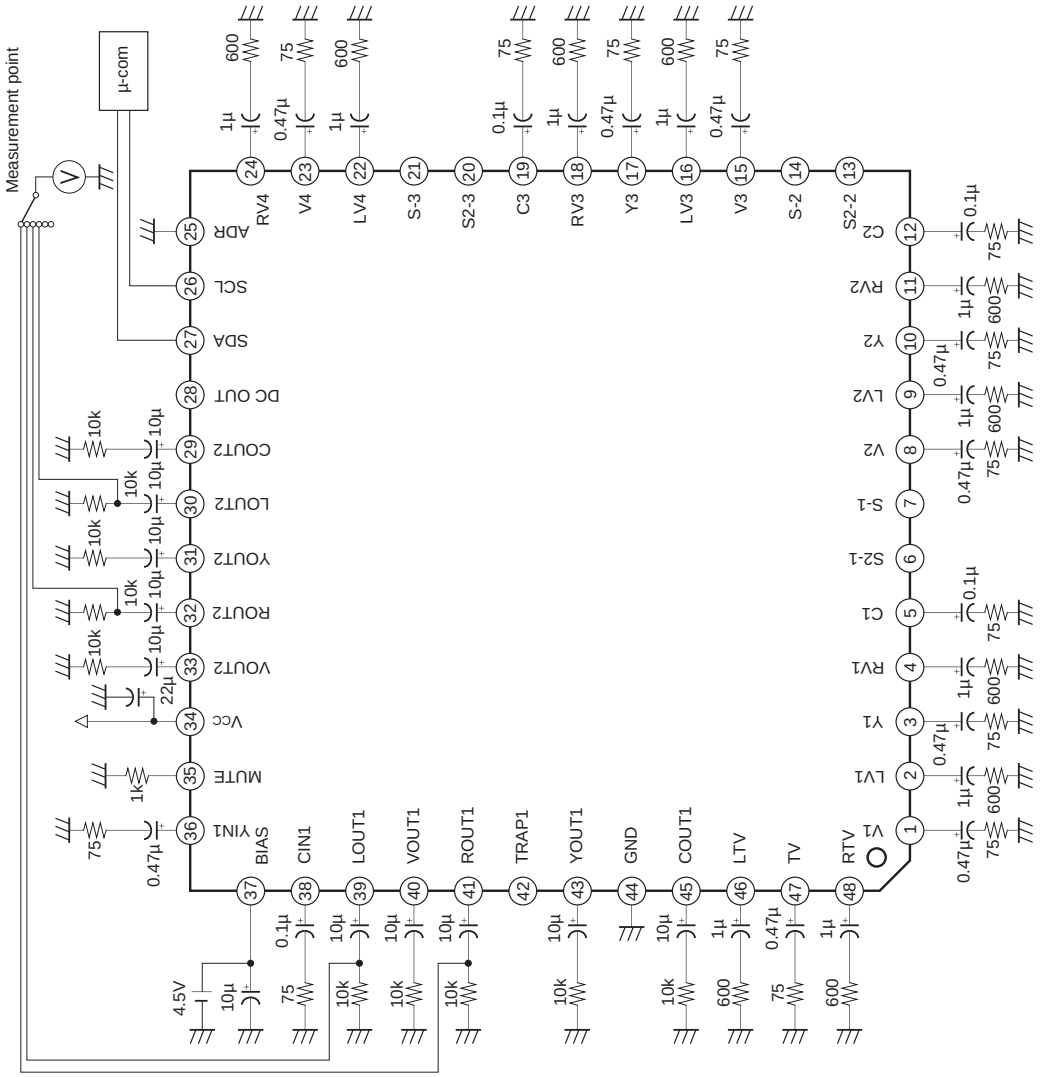


Fig. 5-a. Audio system (residual noise) measurement circuit (CXA2089Q)

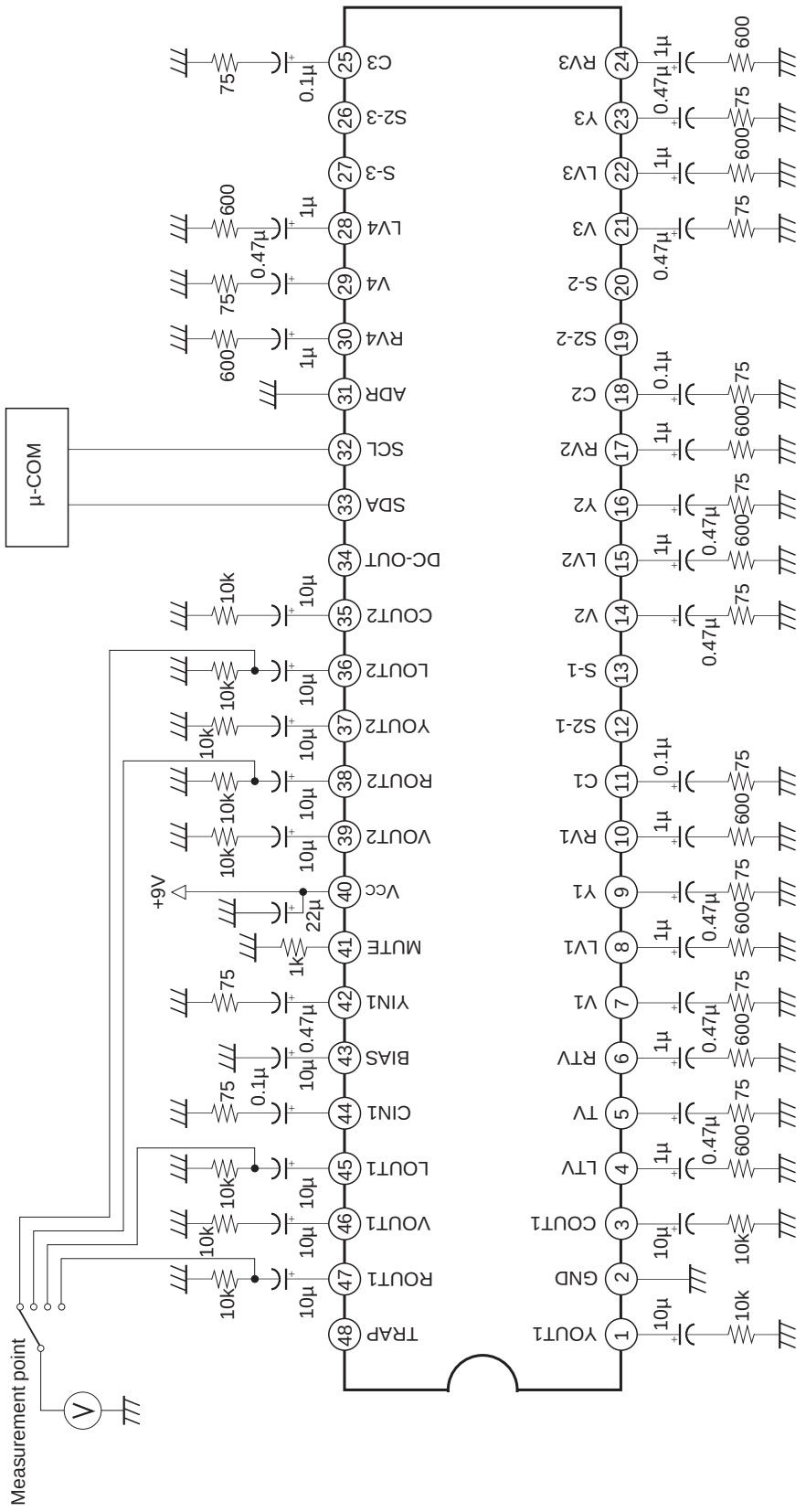


Fig. 5-B. Audio system (residual noise) measurement circuit (CXA2089S)

I²C BUS Control Signal

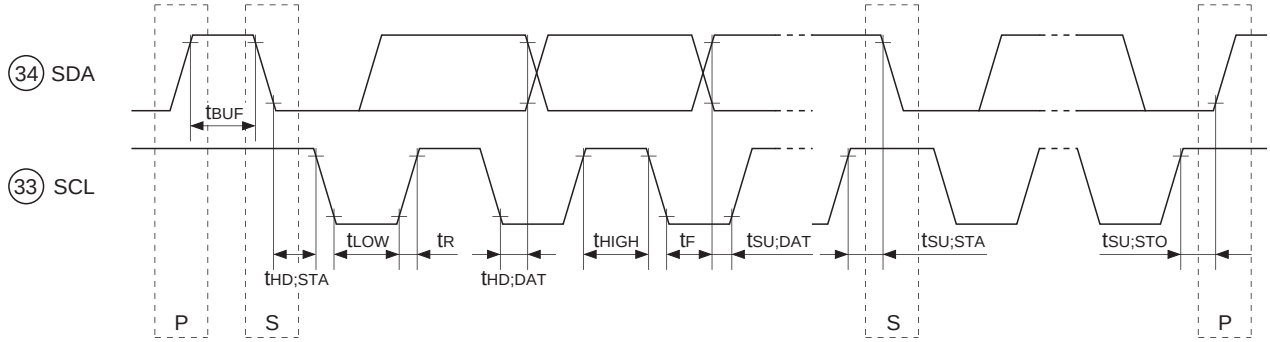


Fig. 6. I²C BUS Control Signal Timing Chart

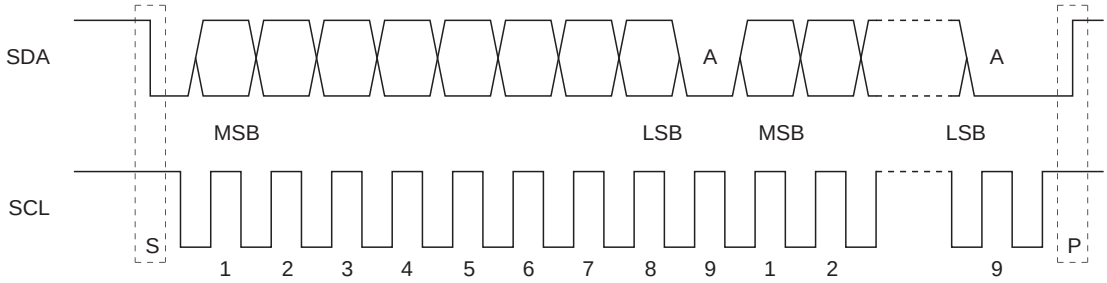
Description of Operation

The CXA2089Q/S is a TV I²C bus-compatible AV switch IC. The video system and the stereo audio system both have 5 inputs and 2 outputs each. 3 of the 5 video system inputs support S2 and S protocols.
The desired inputs can be independently assigned to each output (in the audio system, the left and right channels are processed as one unit) by I²C bus control. However, the same input is assigned to both the video and audio system output 2.

I²C BUS Registers

1) I²C BUS

The I²C bus (inter-IC bus) is an inter-IC bus system developed by Philips. Two lines (SDA – serial data, SCL – serial clock) provide control over start, stop, data transfer, synchronization, and collision avoidance. The IC outputs are either open collector or open drain, forming a bus line in the wired OR format.



S: Start condition; SDA is set "Low" when SCL is "High"
P: Stop condition; SDA is set "High" when SCL is "High"
A: Acknowledge; signal sent from the slave

Data is transmitted by MSB-first. One data unit consists of 8 bits, to which the acknowledge signal, which indicates that the data has been accepted by the slave, is attached at the end. Normally, the slave*1 IC receives data at the rising edge of SCL and the master*2 IC changes data at the falling edge of SCL.

*1 Slave: An IC that is placed under the control of the master. In a normal system, all devices excluding the central microcomputer are slaves.

*2 Master: A central microcomputer or other controlling IC.

2) Control Registers

The CXA2089Q/S control is exercised by writing 2-byte data into the two 8-bit control registers which control the output selector circuits for the 2 outputs.

S	Slave address	A	DATA1	A	DATA2	A	P

S: Start condition
A: Acknowledge
P: Stop condition

Control register structure (DATA1 and DATA2)

- All registers are set to "0" during IC power on.
- "*" indicates undefined.

	b7	b6	b5	b4	b3	b2	b1	b0
Slave add.	1	0	0	1	0	0	ADR	R/W
DATA1	A-GAIN	S/COMP1	V-IN1			A-IN1		
DATA2	*	S/COMP2	AV-IN2			DC OUT		*

R/W (1): Read/write mode
0: Control data write
1: Status register read

ADR (1): This bit sets the slave address set by the address pin.
0: 90H
1: 92H

A-GAIN (1): LOUT1/ROUT1 output gain selector
0: 0dB output
1: –6dB output

S/COMP1 and S/COMP2 (1 each): S terminal input/composite signal input selectors
By setting S/COMP1 to "0", when composite signal input is selected, YOUT1/COUT1 output the inputs from YIN1/CIN1.
0: Composite signal inputs (TV, V1 to V4 inputs)
1: S terminal inputs (Y1/C1 to Y3/C3 inputs)

V-IN1 (3 each): This bit selects the input signals output to each video output.
0: Mute
1: Selects the TV input
2: Selects the V1 and Y1/C1 inputs
3: Selects the V2 and Y2/C2 inputs
4: Selects the V3 and Y3/C3 inputs
5: Selects the V4 inputs
6: Mute
7: Mute

A-IN1 (3 each): This bit selects the input signals output to each audio output.

0: Mute
1: Selects the LTV/RTV inputs
2: Selects the LV1/RV1 inputs
3: Selects the LV2/RV2 inputs
4: Selects the LV3/RV3 inputs
5: Selects the LV4/RV4 inputs
6: Mute
7: Mute

AV-IN2 (3): This bit selects the input signals output to output 2 (VOUT2, YOUT2/COUT2, LOUT2/ROUT2).

Note) Both the video output and the audio output are selected at the same time only for AV-IN2.

0: Mute
1: Selects the TV and LTV/RTV inputs
2: Selects the V1, Y1/C1 and LV1/RV1 inputs
3: Selects the V2, Y2/C2 and LV2/RV2 inputs
4: Selects the V3, Y3/C3 and LV3/RV3 inputs
5: Selects the V4 and LV4/RV4 inputs
6: Mute
7: Mute

DC OUT (2): This bit sets the DC voltage output from DC OUT.

0: 4.5V
1: 0V
2: 1.9V
3: 4.5V

3) Status Registers

• When reading two bytes

S	Slave address	A	DATA1	A	DATA2	NA	P

• When reading one byte

S	Slave address	A	DATA1	NA	P

S: Start condition
A: Acknowledge
NA: No acknowledge
P: Stop condition

When communication is to be terminated in the status register reading mode, the no-acknowledge signal is needed to assure that the master does not issue the acknowledge signal to the slave.
It is possible to read only DATA1 of the status register by sending the no-acknowledge signal after DATA1.

Status register structure (DATA1 and DATA2)

"*" indicates undefined.

	b7	b6	b5	b4	b3	b2	b1	b0
Slave add.	1	0	0	1	0	0	ADR	1
DATA1	S1SEL	S2SEL	S3SEL	*	S-C1		S-C2	
DATA2	$\overline{\text{S1SEL}}$	$\overline{\text{S2SEL}}$	$\overline{\text{S3SEL}}$	*	S-C3		*	

S1SEL to S3SEL (1 each): S-1 to S-3 pin status

0: S-1 to S-3 pins are not grounded.

1: S-1 to S-3 pins are grounded.

S1SEL to S3SEL are actually determined by comparing the S-1 to S-3 pin DC voltages with 3.5V.

S-1 to S-3 pin DC voltage	S1SEL to S3SEL
3.5V or more	0
3.5V or less	1

S-C1, S-C2, S-C3 (2 each): S2-1, S2-2 and S2-3 pin status

0: 4:3 video signal

1: 4:3 letter-box signal

2: 16:9 video squeezed signal

3: No signal

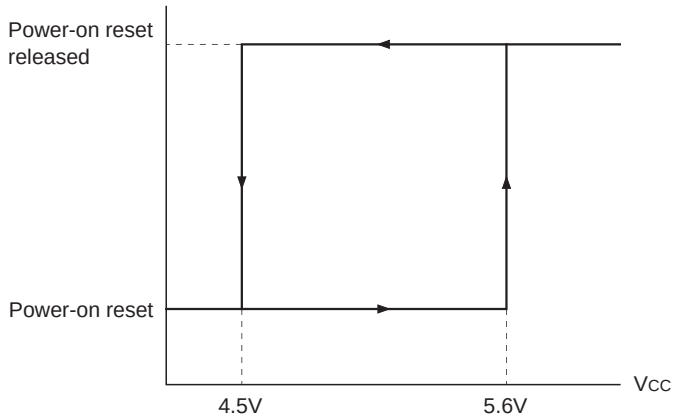
S-C1 to S-C3 are actually determined by comparing the S2-1 to S2-3 pin DC voltages with two threshold. However, when the S-1 to S-3 pins are open, the outputs are fixed to "3".

S2-1 to S2-3 pin DC voltage	S-C1 to S-C3
1.3V or less	0
1.3V or more to 2.5V or less	1
2.5V or more	2
S-1 to S-3 OPEN	3

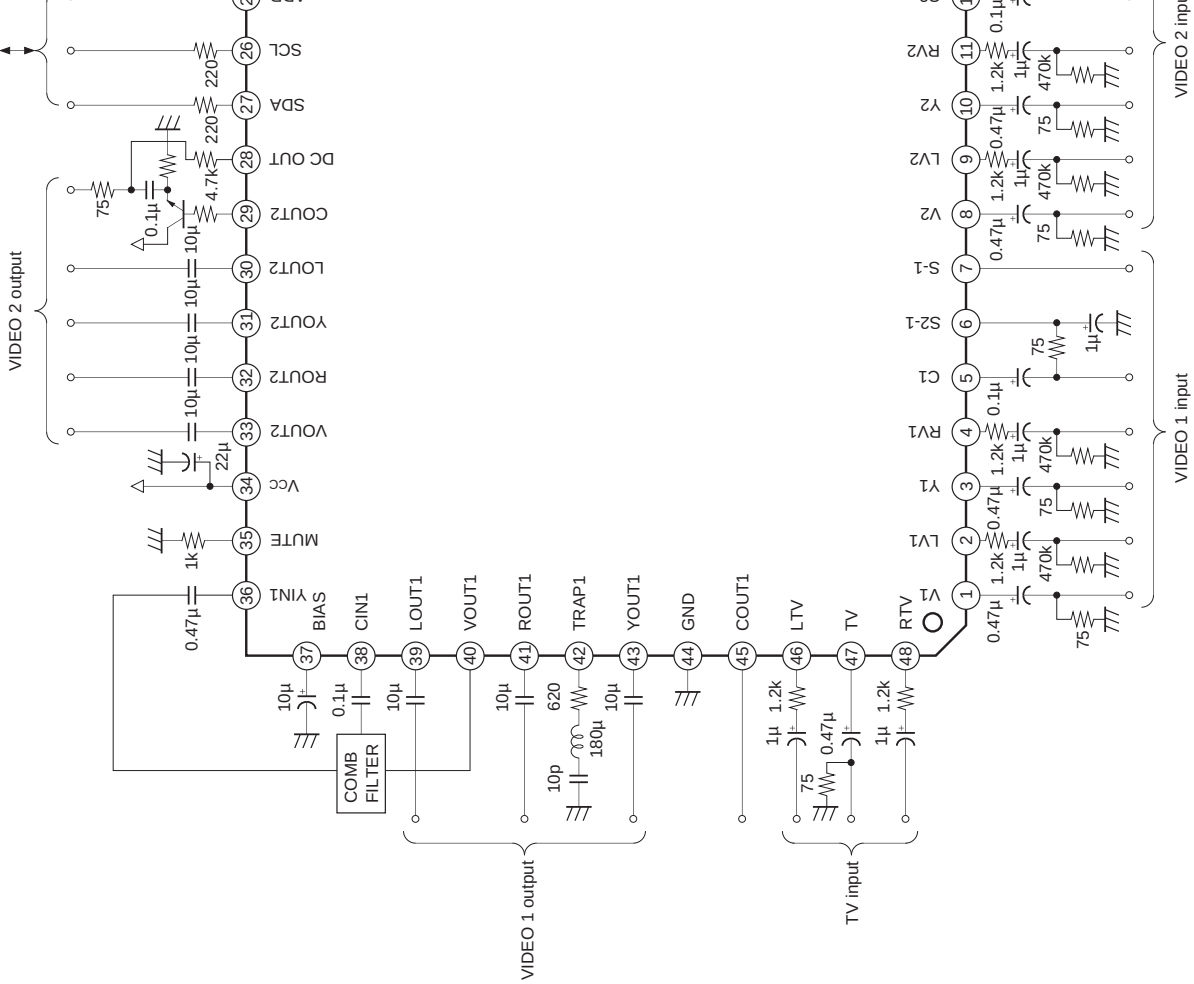
4) Power-on Reset

The CXA2089Q/S has an internal power-on reset function that sets each control register to "0" during IC power ON.

The power-on reset V_{TH} has hysteresis.



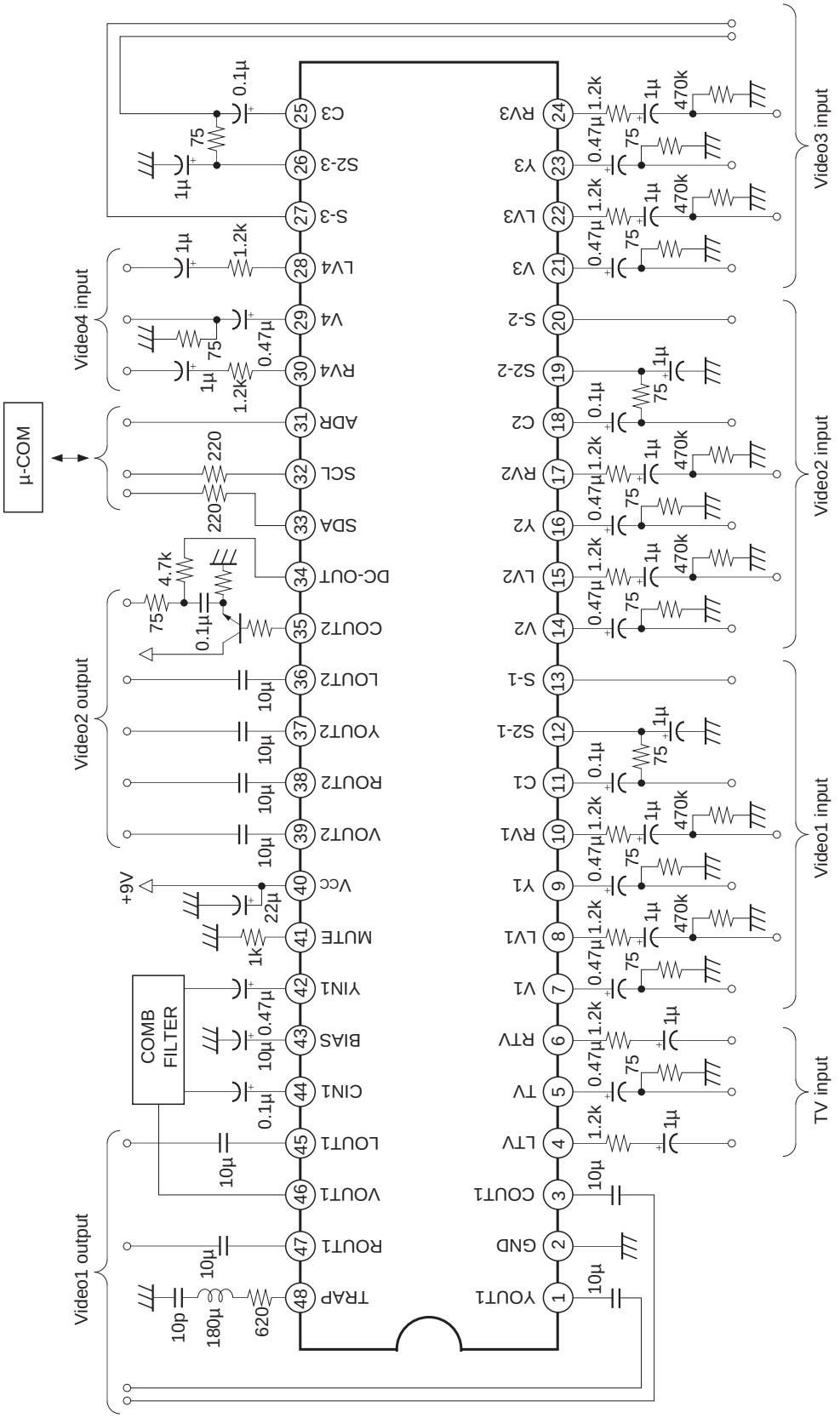
Application Circuit (CXA2089Q)



- Depending on the output bias of the comb filters, pay attention to the polarities of the capacitors since the bias at Pins 36 and 38 is approximately 3.1V and 4.5V, respectively.
- Connect Pin 25 to Vcc when setting the slave address of the IC to 92H.
- The audio output can be muted by setting Pin 35 to 3.5V or more.
- The TRAP (Pin 42) are of 3.58MHz subcarrier.
- Pay attention to the polarities of the capacitors since each output of video system and audio system has optional bias, respectively.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit (CXA2089S)

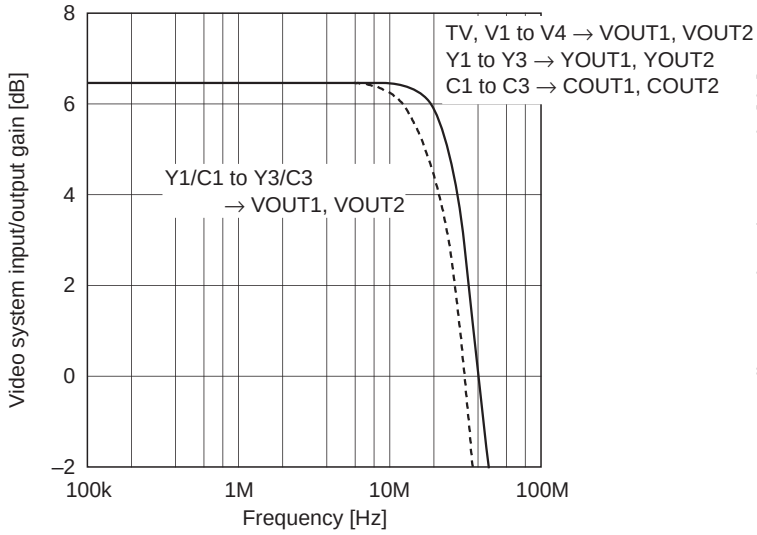


- Depending on the output bias of the comb filters, pay attention to the polarities of the capacitors since the bias at Pins 42 and 44 is approximately 3.1V and 4.5V, respectively.
- Connect Pin 31 to Vcc when setting the slave address of the IC to 92H.
- The audio output can be muted by setting Pin 41 to 3.5V or more.
- The TRAP (Pin 48) are of 3.58MHz subcarrier.
- Pay attention to the polarities of the capacitors since each output of video system and audio system has optional bias, respectively.

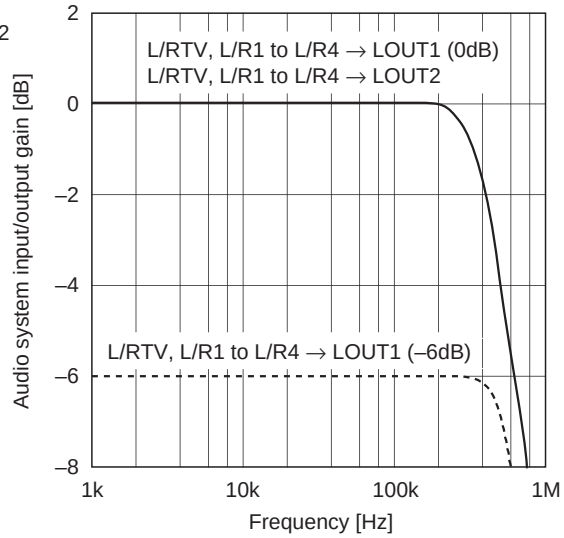
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

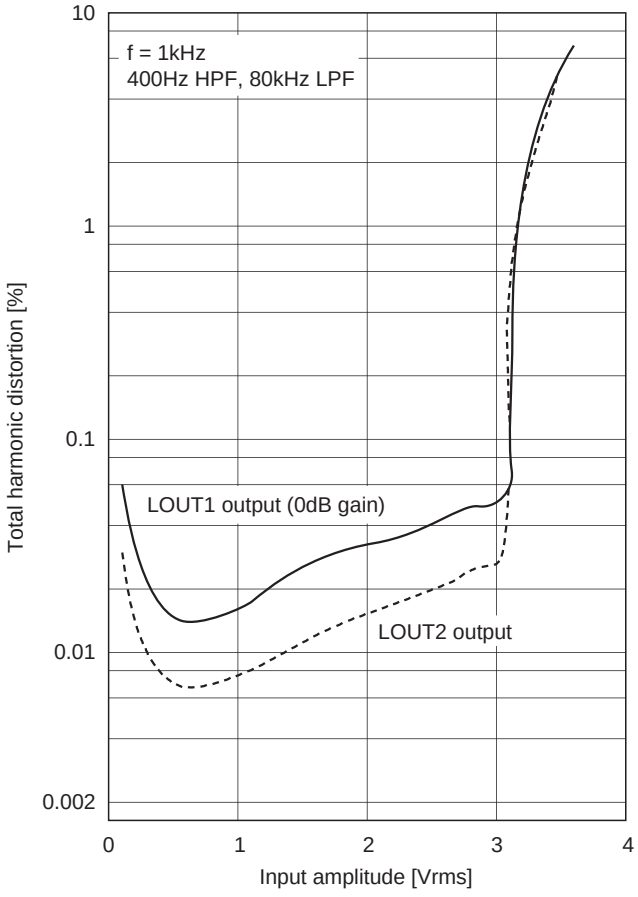
Video system frequency response characteristics



Audio system frequency response characteristics



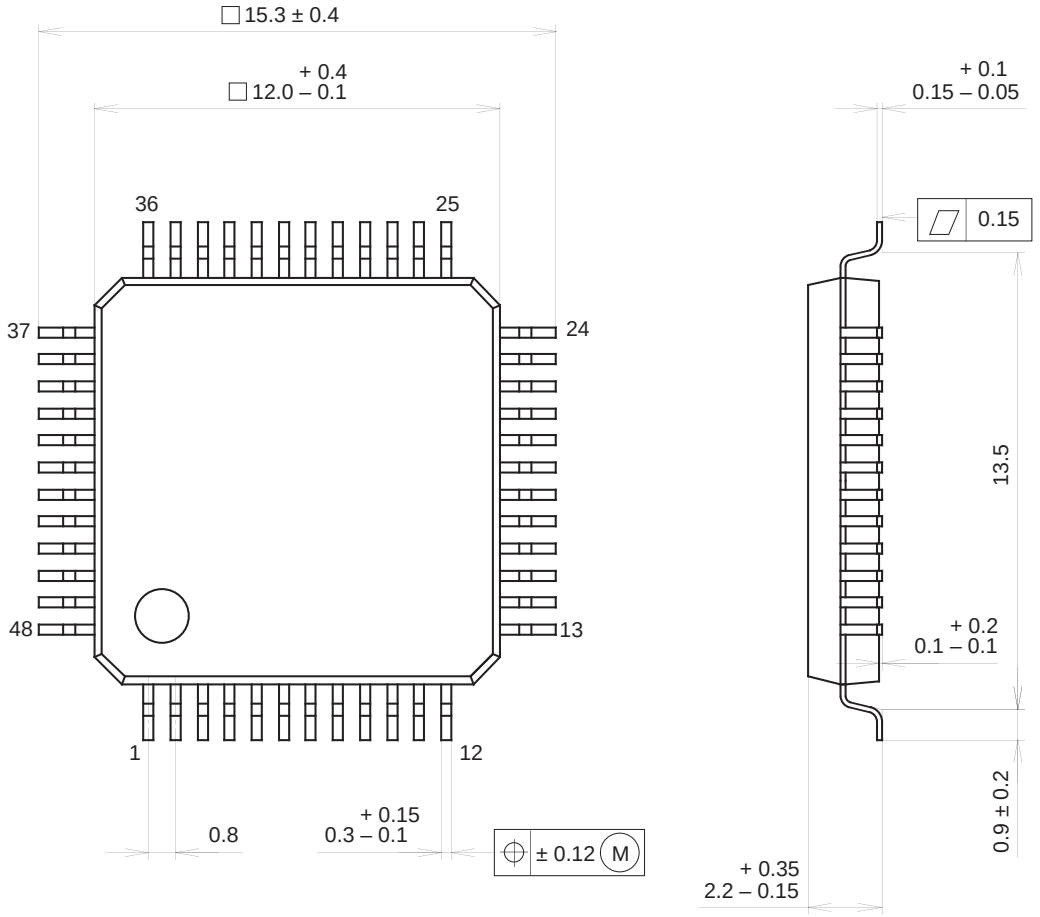
Audio system distortion vs. Input amplitude



Package Outline Unit: mm

CXA2089Q

48PIN QFP (PLASTIC)



SONY CODE	QFP-48P-L04
EIAJ CODE	*QFP048-P-1212-B
JEDEC CODE	————

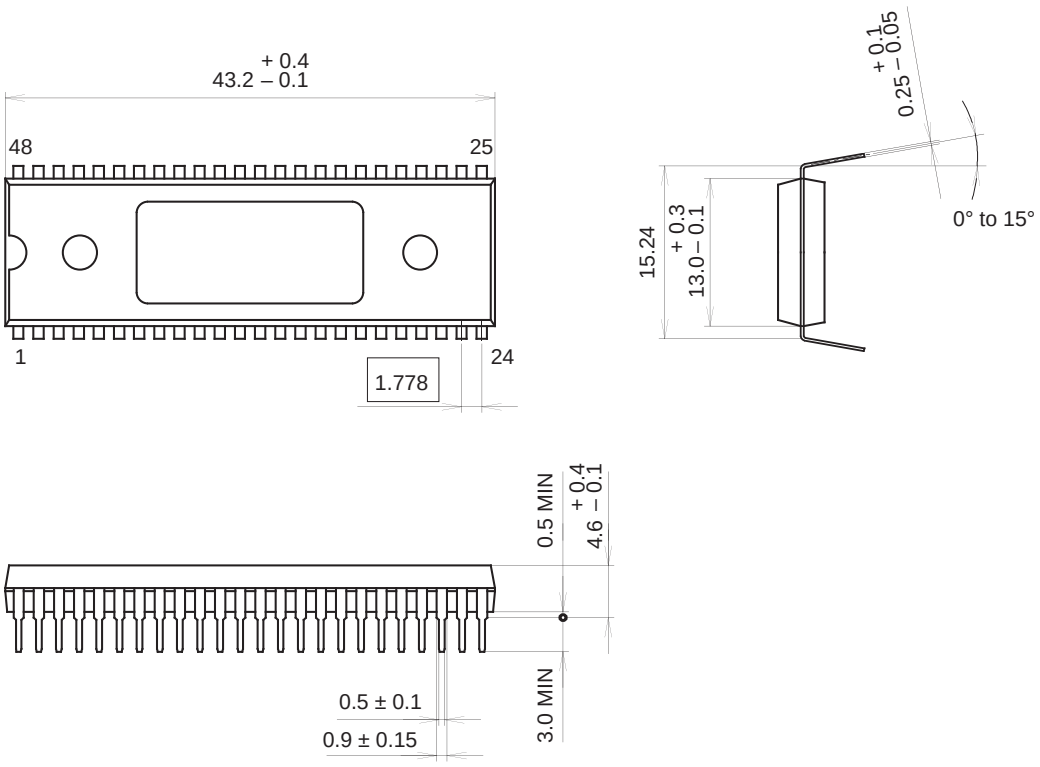
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).

CXA2089S

48PIN SDIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.Center part is mirror surface.

SONY CODE	SDIP-48P-02
EIAJ CODE	SDIP048-P-0600
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	5.1g